**Bug-2 Report**

**Group-5**

1. **Failing Test name**

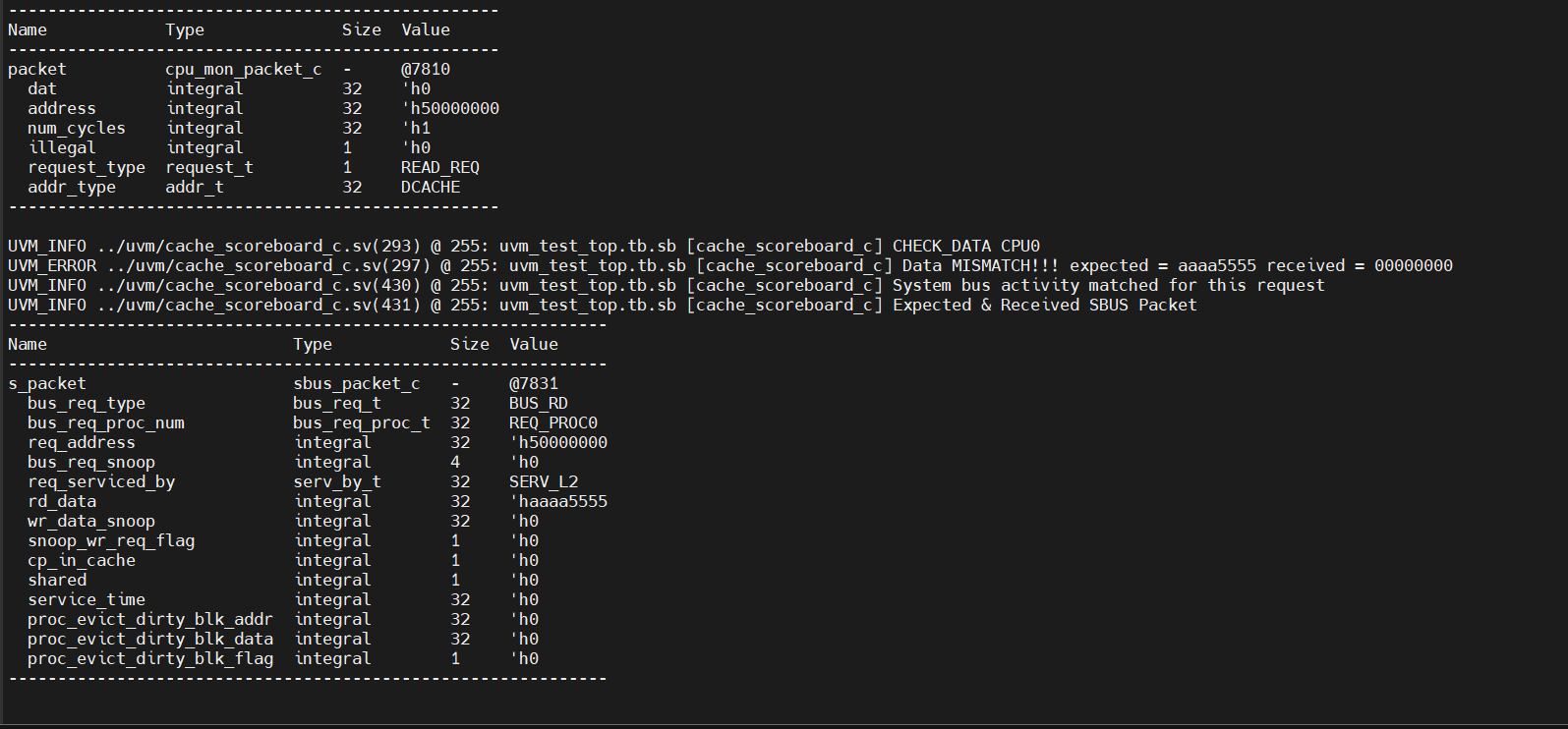
Data cache read Miss Test

1. **Test description (Describe the planned scenario and the expected result)**

read\_miss\_dcache: A basic read on the data cache was executed, and was expected to get data from level-2 cache.

1. **Failing assertion that helped you identify the bug**

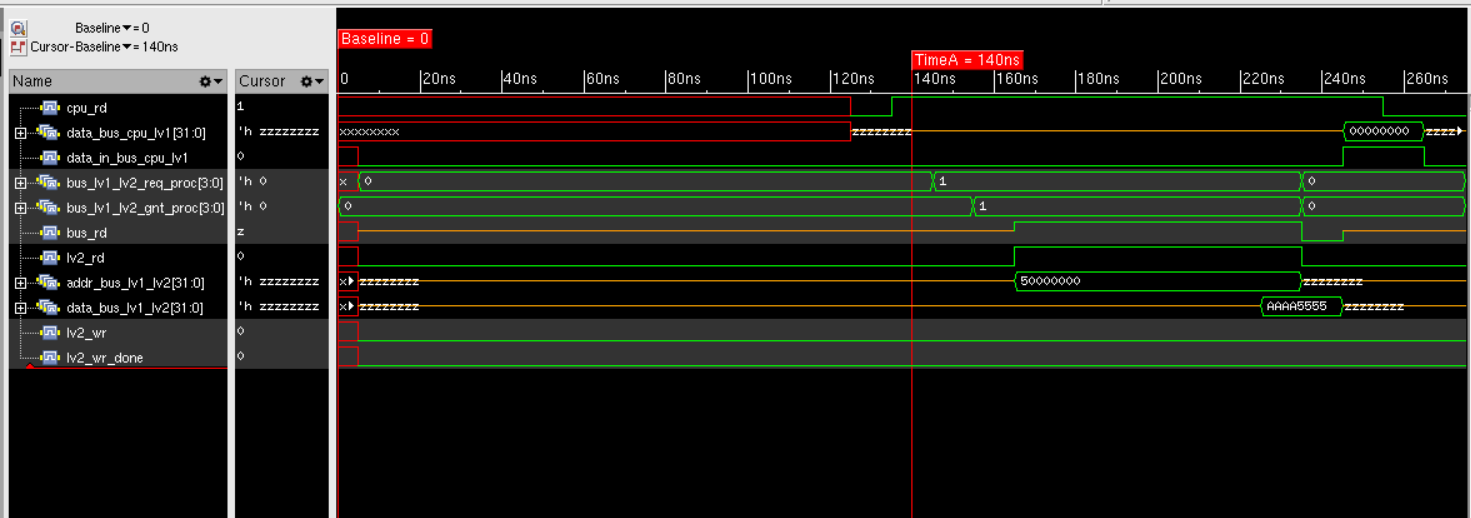
This bug was identified by the scoreboard, since the expected and received values had a mismatch as shown b

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1. **Brief description of diagnosis**

Zero is being received in data\_bus\_cpu\_lv1 even though correct data is present in data\_bus\_lv1\_lv2, so the data is being exchanged wrongly. To correct this, the design files were checked for assignments of data\_bus\_lv1\_lv2 as well as assignments to data\_bus\_cpu\_lv1.

Traced simulation to observe bus\_rd signal:

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1. **Erroneous RTL file name**

main\_func\_lv1\_dl.sv

1. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**

170. cache\_var[{index\_proc, 2’b00}] <= data\_bus\_lv1\_lv2;

1. **Corrected RTL code (only mention the corrections)**

170. cache\_var[{index\_proc, blk\_access\_proc}] <= data\_bus\_lv1\_lv2;